Kajigaya et al.

[45] Date of Patent: * Jan. 9, 1990

[54] **SEMICONDUCTOR MEMORY**

[75] Inventors: Kazuhiko Kajigaya, Kamiyuki Sato, both of Ome-shi, Japan

[73] Assignee: Hitachi, Ltd., Tokyo, Japan

[*] Notice: The portion of the term of this patent subsequent to Oct. 25, 2005 has been disclaimed.

[21] Appl. No.: 388,814

[22] Filed: Oct. 11, 1989

Related U.S. Application Data

[62] Division of Ser. No. 878,073, Jun. 24, 1986, Pat. No. 4,780,855.

[30] **Foreign Application Priority Data**

Jun. 26, 1985 [JP] Japan 60-137793

[51] Int. Cl.* G11C 7/00

[52] U.S. Cl. 365/208; 365/205

[58] Field of Search 365/149, 203, 205, 208, 365/210

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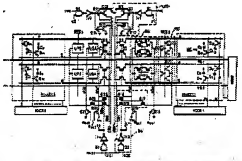
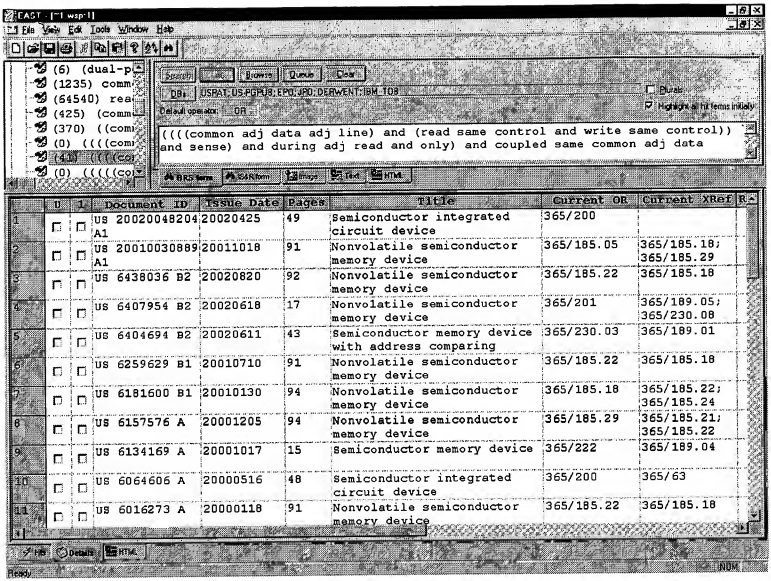
Primary Examiner—Joseph A. Popek
Attorney, Agent, or Firm—Antonelli, Terry & Wands

[57] **ABSTRACT**

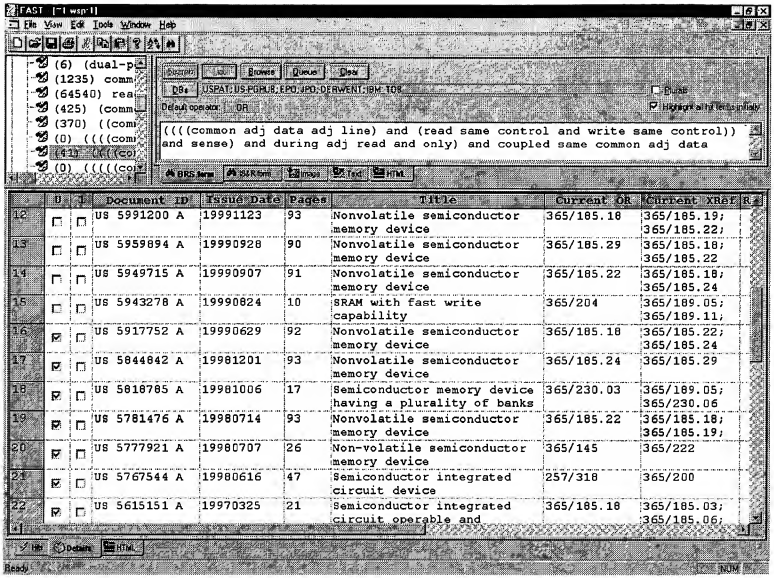
A dynamic RAM is arranged such that a common data line in each of its non-selected ones of the divided memory arrays is connected to a pair of common source lines of a sense amplifier corresponding to the memory array concerned, whereby the potential of the common data line is set at a medium level which is substantially equal to the potential of the data lines by utilizing the medium potential of the pair of common source lines and a relatively large parasitic capacity thereof, thereby maintaining the data lines at the half-precharge level. The pair of common source lines are shorted to each other during the non-select period of the memory arrays, so that the common source lines have a medium level which is substantially equal to the half-precharge level of the data lines.

20 Claim, 3 Drawing Sheets

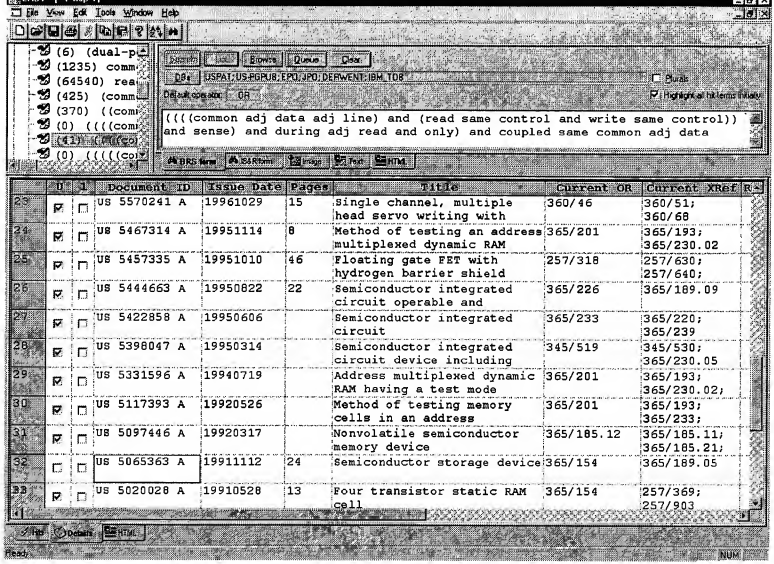


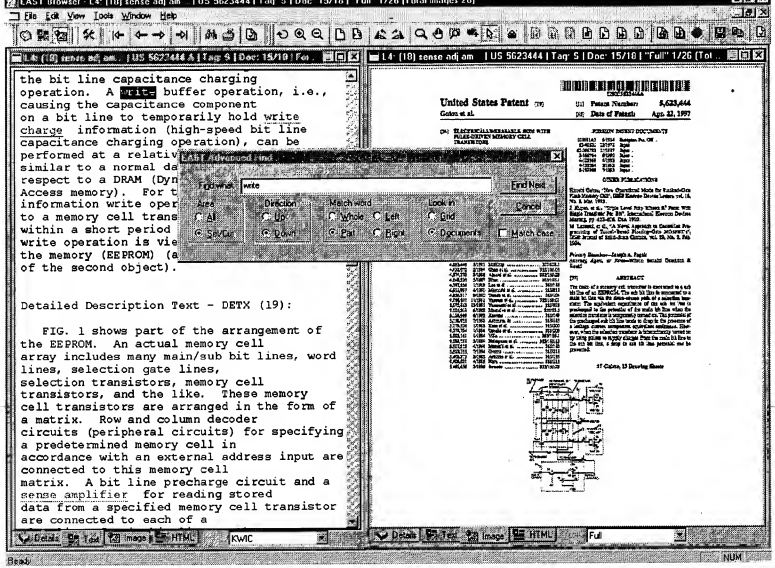


	D	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	☐	☐	US 20020048204 A1	20020425	49	Semiconductor integrated circuit device	365/200		
2	☐	☐	US 20010030889 A1	20011018	91	Nonvolatile semiconductor memory device	365/185.05	365/185.18; 365/185.29	
3	☐	☐	US 6438036 B2	20020820	92	Nonvolatile semiconductor memory device	365/185.22	365/185.18	
4	☐	☐	US 6407954 B2	20020618	17	Nonvolatile semiconductor memory device	365/201	365/189.05; 365/230.08	
5	☐	☐	US 6404694 B2	20020611	43	Semiconductor memory device with address comparing	365/230.03	365/189.01	
6	☐	☐	US 6259629 B1	20010710	91	Nonvolatile semiconductor memory device	365/185.22	365/185.18	
7	☐	☐	US 6181600 B1	20010130	94	Nonvolatile semiconductor memory device	365/185.18	365/185.22; 365/185.24	
8	☐	☐	US 6157576 A	20001205	94	Nonvolatile semiconductor memory device	365/185.29	365/185.21; 365/185.22	
9	☐	☐	US 6134169 A	20001017	15	Semiconductor memory device	365/222	365/189.04	
10	☐	☐	US 6064606 A	20000516	48	Semiconductor integrated circuit device	365/200	365/63	
11	☐	☐	US 6016273 A	20000118	91	Nonvolatile semiconductor memory device	365/185.22	365/185.18	



	D	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
12	☐	☐	US 5991200 A	19991123	93	Nonvolatile semiconductor memory device	365/185.18	365/185.19; 365/185.22;	
13	☐	☐	US 5959894 A	19990928	90	Nonvolatile semiconductor memory device	365/185.29	365/185.18; 365/185.22	
14	☐	☐	US 5949715 A	19990907	91	Nonvolatile semiconductor memory device	365/185.22	365/185.18; 365/185.24	
15	☐	☐	US 5943278 A	19990824	10	SRAM with fast write capability	365/204	365/189.05; 365/189.11;	
16	☑	☐	US 5917752 A	19990629	92	Nonvolatile semiconductor memory device	365/185.18	365/185.22; 365/185.24	
17	☑	☐	US 5844842 A	19981201	93	Nonvolatile semiconductor memory device	365/185.24	365/185.29	
18	☑	☐	US 5818785 A	19981006	17	Semiconductor memory device having a plurality of banks	365/230.03	365/189.05; 365/230.06	
19	☑	☐	US 5781476 A	19980714	93	Nonvolatile semiconductor memory device	365/185.22	365/185.18; 365/185.19;	
20	☑	☐	US 5777921 A	19980707	26	Non-volatile semiconductor memory device	365/145	365/222	
21	☑	☐	US 5767544 A	19980616	47	Semiconductor integrated circuit device	257/318	365/200	
22	☑	☐	US 5615151 A	19970325	21	Semiconductor integrated circuit operable and	365/185.18	365/185.03; 365/185.06;	

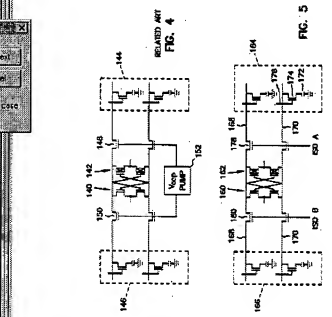




further comprises a shared p-sense amplifier, a shared n-sense amplifier, and a plurality of n-channel depletion transistors selectively coupling the plurality of pairs of digit lines to the shared p-sense amplifier and the n-sense amplifier.

Detailed Description Text - DETX (3):

In the most general sense, a memory circuit comprises memory cells which store data. Depending upon the type of memory, this data can be read, or read and written. That is, some memories are read-only while others allow data to be read, manipulated, and re-written. Because many types of memories store data as a charge on a capacitor, sense amplifiers are implemented to detect small charges and amplify the charge for further processing. FIG. 1 is a simplified block diagram of a memory array 100 having memory cells 101 connected to a sense amplifier 102. The sense amplifier can be used to sense a charge stored on the memory cells and write the charge back to the memory



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[73] Assignee: Hitachi, Ltd., Tokyo, Japan

[21] Appl. No.: 878,071

[22] Filed: Jun. 24, 1986

[30] Foreign Application Priority Data

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[51] Int. Cl.4 ..... G11C 7/00

[52] U.S. Cl. 365/205; 365/205

[58] Field of Search 365/149, 203, 204, 205, 365/210

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18 Claims, 9 Drawing Sheets